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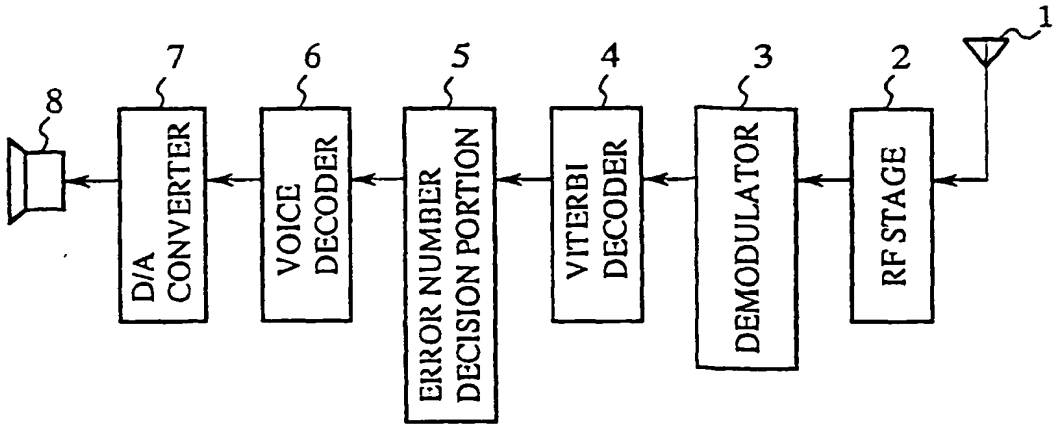
(54) Error detecting device

(57) An error detecting device for received digital data is provided which solves a problem of a conventional device in that error detection following the Viterbi decoding performed on most important bits cannot detect all errors if they include a considerable amount of errors. The present error detecting device includes a Viterbi decoder (4) for carrying out the Viterbi decoding of the received digital data, an error number decision portion (5) for comparing a threshold value with the number of errors of the path metric obtained by the Viterbi decoding, and a voice decoder (6) for decoding the received digital data, on which the error number decision portion (5) decides that the number of errors is below the threshold value.

FIG.1



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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to an error detecting device of received digital data such as voice data, image data, character data or control data handled on a frame by frame basis.

Description of Related Art

[0002] Fig. 8 is a block diagram showing a configuration of a receiver of a conventional digital portable telephone with an error detecting device of received digital data arranged in frames. In Fig. 8, the reference numeral 101 designates an antenna, 102 designates an RF stage for accepting a received signal through the antenna 101, 103 designates a demodulator, 104 designates a Viterbi decoder, 105 designates a CRC (Cyclic Redundancy Check) decision portion as an error detector, 106 designates a voice decoder, 107 designates a D/A (Digital/Analog) converter, and 108 designates a speaker, which are connected in this order.

[0003] Next, the operation of the conventional device will be described with reference to the flowchart of Fig. 9.

[0004] Received digital data obtained through the antenna 101, RF stage 102 and demodulator 103 is fed to the Viterbi decoder 104 which carries out error correcting of a voice frame or the like at step ST7-1. Subsequently, the CRC decision portion 105 carries out at step ST7-2 error detection of only most important bits which will be described later. If a decision is made that the received digital data is correct, the voice decoder 106 performs decoding at step ST7-3, and operates the speaker 108 through the D/A converter 107. In contrast, if a decision is made that the received digital data is incorrect, the voice decoder 106 carries out post-error-detecting processing such as mute processing of the voice data at step ST7-4, in which case the D/A converter 107 does not operate the speaker 108.

[0005] With such a configuration, the conventional error detecting device of the received digital data performs error detection of only the most important bits after the Viterbi decoding. It sometimes, however, miss detecting a considerable number of errors occurred in the most important bits, resulting in odd sounds produced from the speaker 108 through decoding of the voice data. For example, with regard to the full rate voice frame of the GSM (Global System for Mobile Communications) system, the CRC portion miss many errors occurred in the most important bits because it performs the error detection on the basis of parity bits consisting of only three bits, and hence its probability is rather low.

[0006] The full rate voice frame in the GSM is 20 ms in length, and consists of 260 information bits which are divided into important 182 class-1 bits which undergo error correction, and 78 class-2 bits which do not undergo the error correction. The 182 class-1 bits are further divided into the most important 50 class-1a bits and 132 class-1b bits, and only the most important 50 class-1a bits are subjected to the error detection, that is, the CRC decision.

[0007] Thus, the CRC decision portion 105 passes the information bits through a divider to make a decision that no error has occurred if the remainders in the transmitter and receiver match each other, or that some error has occurred if they do not match, in which case the mute processing is carried out. Sometimes, however, because of an error of the parity bits themselves during the transmission, the CRC computed by the receiver can match the CRC generated by the transmitter, even if they must be actually different from each other. In this case, the odd sounds result from the decoding of the voice data.

[0008] The probability of such erroneous detection depends on the number of bits of the parity bits of the CRC decision portion 105. For example, when the parity bits consists of three bits, the probability of making a wrong decision becomes 1/8=12.5% in the worst case.

SUMMARY OF THE INVENTION

[0009] The present invention is implemented to solve the foregoing problem. It is therefore an object of the present invention to provide a error detecting device of the received digital data which can detect their errors at high accuracy.

[0010] According to a first aspect of the present invention, there is provided an error detecting device of received digital data comprising: a Viterbi decoder for carrying out Viterbi decoding of the received digital data frame by frame; an error number decision portion for comparing a number of errors of a path metric of the Viterbi decoding with a predetermined threshold value; and a decoder for decoding the received digital data, on which the error number decision portion makes a decision that the number of errors of the path metric is equal to or less than the threshold value.

[0011] According to a second aspect of the present invention, there is provided an error detecting device of received digital data comprising: a Viterbi decoder for carrying out Viterbi decoding of the received digital data frame by frame; an error number decision portion for comparing a number of errors of a path metric of the Viterbi decoding with a predetermined threshold value; an error detector for detecting an error of at least part of the received digital data, on which the error number decision portion makes a decision that the number of errors of the path metric is equal to or less than the threshold value; and a decoder for decoding the received digital data, on which the error detector makes a decision that a number of errors is equal to or less

than a predetermined value.

[0012] Here, the received digital data may be one of voice data, image data, character data and control data.

[0013] The error detector may consist of a CRC (cyclic redundancy check) detector.

[0014] The threshold value may be preset at a value associated with a number of bits subjected to error correction in each frame.

[0015] The received digital data may consist of a combination of at least two types of data selected from voice data, image data, character data and control data.

[0016] The threshold value may be preset at a value in a range from 5% to 20% of the number of bits subjected to the error correction.

[0017] According to the present invention, the error of the received digital data is detected by comparing the threshold value with the number of errors of the path metrics of the Viterbi decoding, which has high correlation with the error rate of the path metric. This offers an advantage of implementing highly accurate, effective error detection.

[0018] In addition, detecting the error once again of the received digital data which has been decided as including only a small number of errors as a result of the foregoing comparison also has an advantage of achieving highly accurate, effective error detection.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019]

Fig. 1 is a block diagram showing an embodiment 1 of a receiver of a digital portable telephone with an error detecting device of received digital data in accordance with the present invention;

Fig. 2 is a block diagram showing the Viterbi decoder in Fig. 1;

Fig. 3 is a flowchart illustrating the operation of the embodiment 1;

Fig. 4 is a block diagram showing an embodiment 2 of a receiver of a digital portable telephone with an error detecting device of received digital data in accordance with the present invention;

Fig. 5 is a flowchart illustrating the operation of the embodiment 2;

Fig. 6 is a table showing correlations between the number of errors of input data and the number of errors of path metrics;

Fig. 7 is a table showing correlations between error rates and the number of errors of output data;

Fig. 8 is a block diagram showing a configuration of a receiver of a digital portable telephone with a conventional error detecting device of received digital data; and

Fig. 9 is a flowchart illustrating the operation of the conventional system.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0020] The invention will now be described with reference to the accompanying drawings.

EMBODIMENT 1

[0021] Fig. 1 is a block diagram showing an embodiment 1 of a receiver of a digital portable telephone with an error detecting device of received digital data in accordance with the present invention. In Fig. 1, the reference numeral 1 designates an antenna, 2 designates an RF (Radio Frequency) stage for accepting a received signal through the antenna 1, 3 designates a demodulator, 4 designates a Viterbi decoder, 5 designates an error number decision portion, 6 designates a voice decoder (decoder), 7 designates a D/A converter, and 8 designates a speaker, which are connected in this order.

[0022] Fig. 2 is a block diagram showing a configuration of the Viterbi decoder 4. The Viterbi decoder 4 comprises a branch metric calculator 41 for receiving received digital data and performing branch metric calculation; an ACS (add compare select) portion 42 for choosing survivor paths; a path memory 43 for storing the survivor paths of respective states or their corresponding information sequences; and a path metric memory 44 for storing their metrics.

[0023] The branch metric calculator 41 finds the distance of the m-th subsequence of the received sequence for all branches connecting m-th stage states to the (m+1)-th stage states of the trellis of the Viterbi algorithm. The ACS portion 42 adds these distances to the metrics of the m-th stage states to obtain the metric candidates for the (m+1)-th stage states, compares the metric candidates, and selects the minimum of the metric candidates for each state at the (m+1)-th stage as a survivor path. The path memory 43 stores the survivor paths or information sequences corresponding to these survivor paths. The path metric memory 44 stores the number of errors of each path metric, which is defined as the sum total of the distances of respective branches constituting the path metric. Details of the Viterbi algorithm are described, for example, in pp. 486-488 and 786-788 of "Communication Systems Engineering" by John G. Proakis and Masoud Salehi, Prentice-Hall, Inc. 1994, which is incorporated here by reference.

[0024] Next, the operation of the present embodiment 1 will be described with reference to the flowchart of Fig. 3.

[0025] The received digital data obtained through the antenna 1, RF stage 2 and demodulator 3 is supplied to the branch metric calculator 41 of the Viterbi decoder 4, which performs the branch metric calculation. Subsequently, the ACS portion 42 carries out the addition and comparison as described above, and selects the survivor paths. The path memory 43 stores the survivor

paths of the individual states, or the information sequences corresponding the survivor paths. The path metric memory 44 stores the number of errors of the path metrics. Thus, the Viterbi decoding is carried out at step ST3-1.

[0026] The inventors of the present invention experimentally found that the number of errors of the path metric has strict correlation with the number of errors of the input data. Fig. 6 shows an example of the correlations between these numbers, in which the "total number of bits" refers to the number of bits in each frame which are subjected to the error correction. As shown in Fig. 6, the number of errors of the path metric is almost equal to the number of errors of the input data. This supports that the error rate can be detected by means of the number of errors of the path metric obtained by the Viterbi decoding.

[0027] Afterward, the error number decision portion 5 compares the number of errors of the path metric stored in the path metric memory 44 with the predetermined threshold value at step ST3-2, and if the number of errors is greater than the threshold value, the voice decoder 6 carries out post-error-detection processing like the mute processing at step ST3-3.

[0028] On the other hand, if the number of errors of the path metric is less than the threshold value because of a small number of errors in the received digital data, the voice decoder 6 carries out the voice decoding at step ST3-4.

[0029] The threshold value is adjusted in accordance with the types of the received digital data such as image data, voice data sent from a portable telephone because the number of bits subjected to the error correction varies depending on the types of the received digital data. The threshold value is generally set at 5-20% of the number of bits subjected to the error correction.

[0030] Fig. 7 shows experimentally obtained relationships between the number of bits of the input data, the error rate of the input data, and the number of errors of the output data, where the error rate is defined as 100(the number of errors of the input data)/(the number of the bits). As shown in Fig. 7, the number of errors of the output data is zero as long as the error rate is below 10% because of the error correcting function. However, errors in the output data begin to occur in the range from 10% to 15%, and hence the optimum values of the threshold is found to be 10-15% from this experimental results.

[0031] Thus, the present embodiment 1 detects the error of the received digital data by comparing the threshold value with the number of errors of the path metric of the Viterbi decoding, which has close correlation with the error rate of the input data. This has an advantage of achieving accurate, effective error detection of the received digital data.

EMBODIMENT 2

[0032] Fig. 4 is a block diagram showing an embodiment 2 of the receiver of the digital portable telephone with the error detecting device of the received digital data in accordance with the present invention, in which the portions corresponding to those of Fig. 1 are designated by the same reference numerals and the description thereof is omitted here.

[0033] In Fig. 4, the reference numeral 9 designates a CRC decision portion connected between the error number decision portion 5 and voice decoder 6. The CRC decision portion 9 detects again the error of the received digital data, on which a decision has been made by the error number decision portion 5 that the number of errors is below the threshold value.

[0034] Next, the operation of the present embodiment 2 will be described with reference to the flowchart of Fig. 5.

[0035] The received digital data obtained through the antenna 1, RF stage 2 and demodulator 3 is subjected to the Viterbi decoding at step ST5-1. Then, the error number decision portion 5 compares the number of errors of the path metric with the predetermined threshold value at step ST5-2, and if it decides that the number of errors is greater than the threshold value, the voice decoder 6 carries out the post-error-detection processing like the mute processing at step ST5-4.

[0036] On the other hand, if the error number decision portion 5 makes a decision that the number of errors of the path metric is equal to or less than the threshold value, the CRC decision portion 9 detects the error of the received digital data at step ST5-3. If the CRC decision portion 9 detects any error, the voice decoder 6 carries out the post-error-detection processing at step ST5-4. In contrast, if the CRC decision portion 9 does not detect any errors, the voice decoder 6 carries out the voice decoding at step ST5-5.

[0037] Thus, the present embodiment 2 detects the error of the received digital data twice: First, the error number decision portion 5 detects it by comparing the threshold value with the number of errors of the path metric after the Viterbi decoding; and second, the CRC decision portion 9 detects it again using the CRC. This has an advantage of further improving the accuracy of the error detection and decoding.

EMBODIMENT 3

[0038] Although the foregoing embodiments 1 and 2 handle the received digital data of the voice in the digital portable telephone, the received digital data of any type can be handled in the same way as long as they are transmitted on the frame by frame basis. For example, the image data, character data or control data can be processed in the same manner, providing the same effect and advantage of the foregoing embodiments.

Claims

1. An error detecting device for processing received digital data comprising:

   a Viterbi decoder (4) for carrying out Viterbi decoding of the received digital data frame by frame;

   an error number decision circuit (5) for comparing the number of errors of a path metric of the Viterbi decoding with a predetermined threshold value; and

   a decoder (6) for decoding the digital data received from the error number decision circuit (5) after having made the decision that the number of errors of the path metric is equal to or less than the threshold value.

2. An error detecting device for processing received digital data comprising:

   a Viterbi decoder (4) for carrying out Viterbi decoding of the received digital data frame by frame;

   an error number decision circuit (5) for comparing the number of errors of a path metric of the Viterbi decoding with a predetermined threshold value;

   an error detector (9) for detecting an error of at least part of the digital data received from the error number decision portion (5) after having made the decision that the number of errors of the path metric is equal to or less than the threshold value; and

   a decoder (6) for decoding the received digital data, on which the error detector (9) makes the decision that the number of errors is equal to or less than a predetermined value.

3. The error detecting device of Claim 2, wherein said error detector (9) consists of a CRC (cyclic redundancy check) detector.

4. The error detecting device of Claim 1, 2 or 3, wherein said threshold value is preset at a value corresponding to a number of bits subjected to error correction in each frame.

5. The error detecting device of Claim 4, wherein said threshold value is preset to a value of from 5% to 20% of the number of bits subjected to the error correction.

6. The error detecting device of any one of the Claims 1 to 5, wherein said received digital data consists of a combination of at least two types of data selected from voice data, image data, character data and control data.

FIG.1

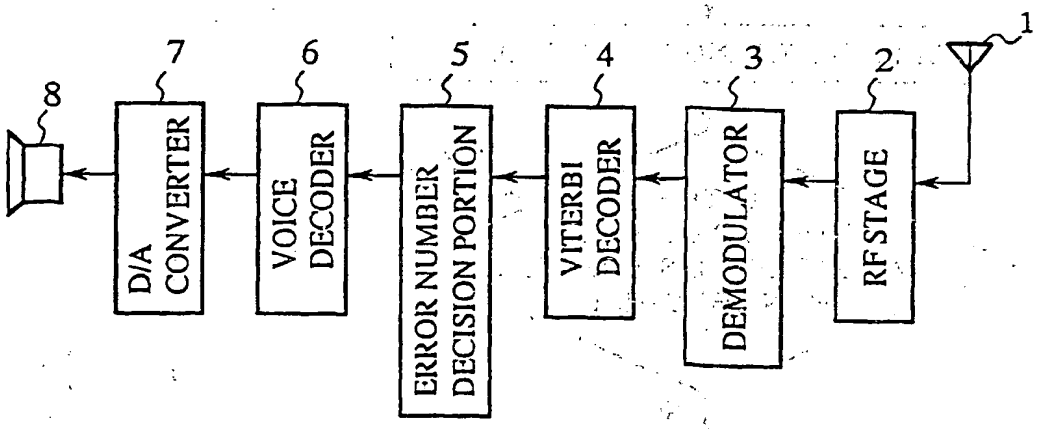

FIG.2

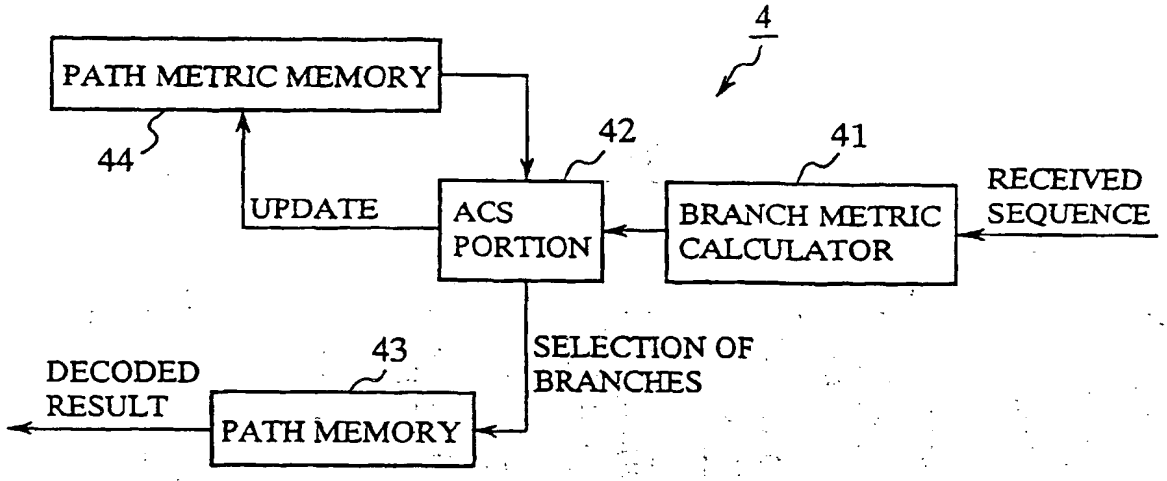

FIG.3

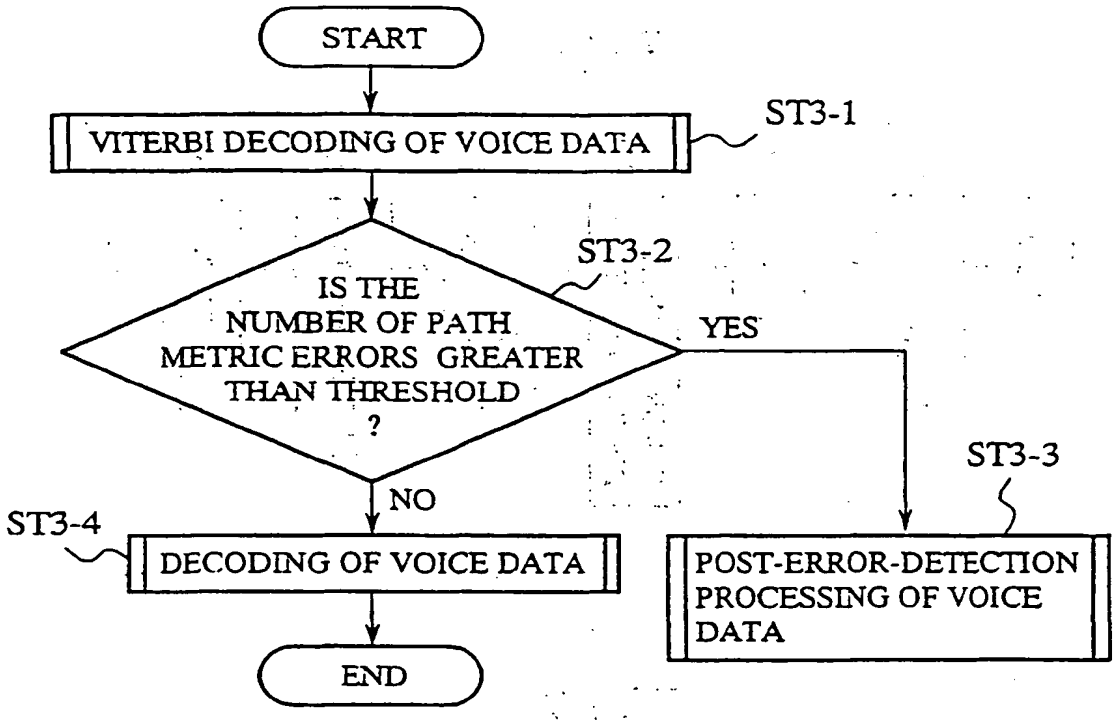
START
VITERBI DECODING OF VOICE DATA
ST3-1
ST3-2
IS THE NUMBER OF PATH METRIC ERRORS GREATER THAN THRESHOLD ?
YES
NO
ST3-3
ST3-4
DECODING OF VOICE DATA
POST-ERROR-DETECTION PROCESSING OF VOICE DATA
END

FIG.4

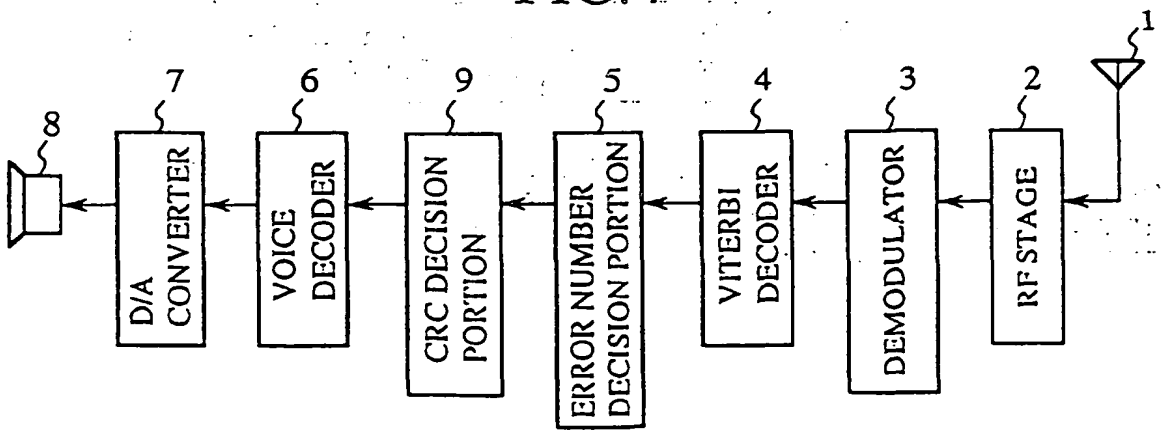
1
2
3
4
5
6
7
8
9
RF STAGE
DEMODULATOR
VITERBI DECODER
ERROR NUMBER DECISION PORTION
CRC DECISION PORTION
VOICE DECODER
D/A CONVERTER

FIG.5

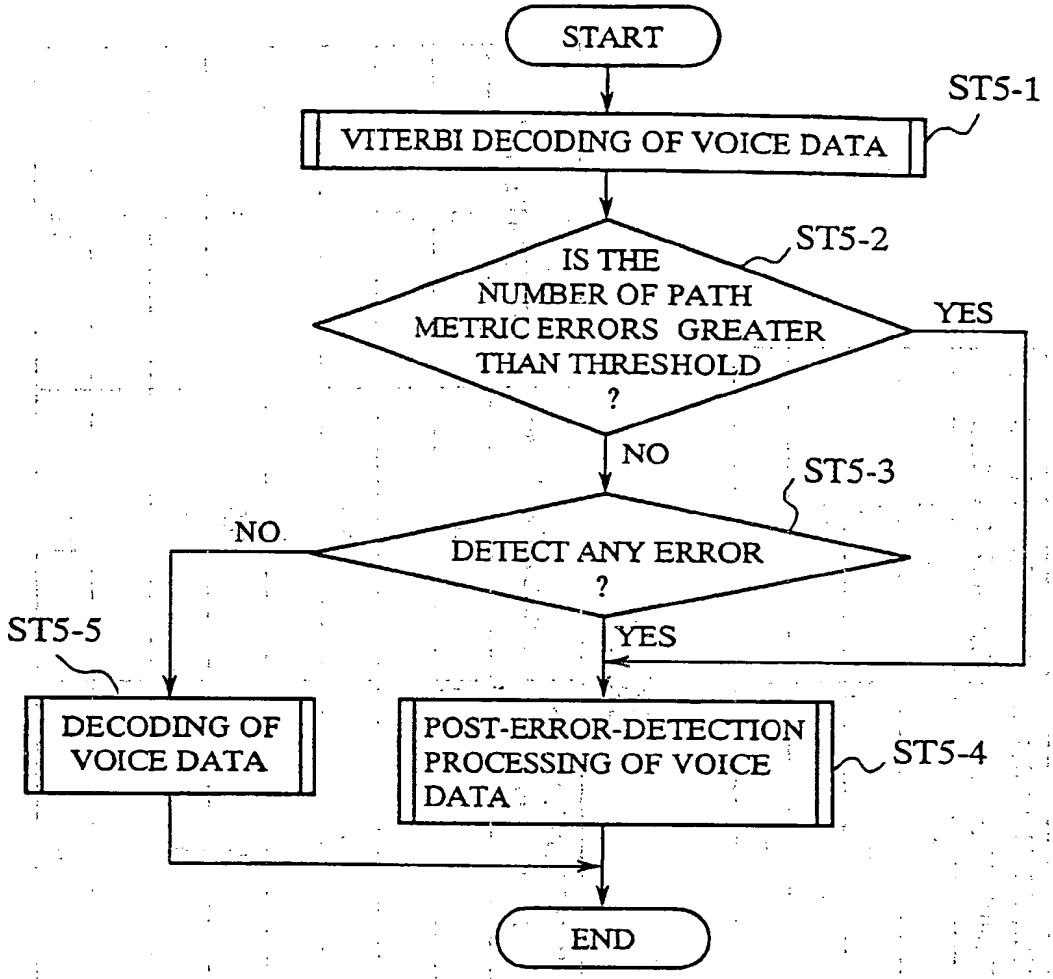

FIG.8 (PRIOR ART)

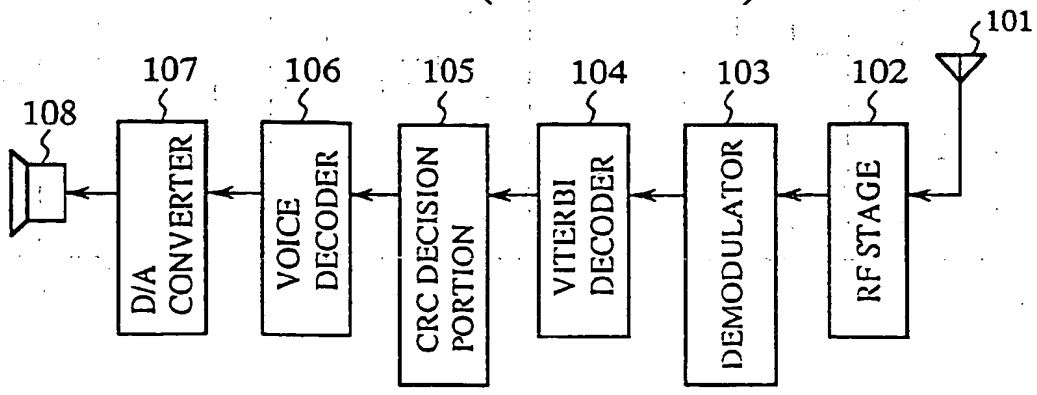

FIG.6

TOTAL NUMBER OF BITS	NUMBER OF ERRORS OF INPUT DATA	NUMBER OF ERRORS OF PATH METRIC
378	0	0
378	10	10
378	20	20
378	30	31

FIG.7

TOTAL NUMBER OF BITS	NUMBER OF ERRORS OF INPUT DATA	ERROR RATE [%]	NUMBER OF ERRORS OF OUTPUT DATA
378	0	0	0
378	10	2.6	0
378	20	5.3	0
378	30	8.0	0
378	40	10.5	0
378	50	13.2	5
378	60	15.8	23
378	70	18.5	72

FIG.9
(PRIOR ART)

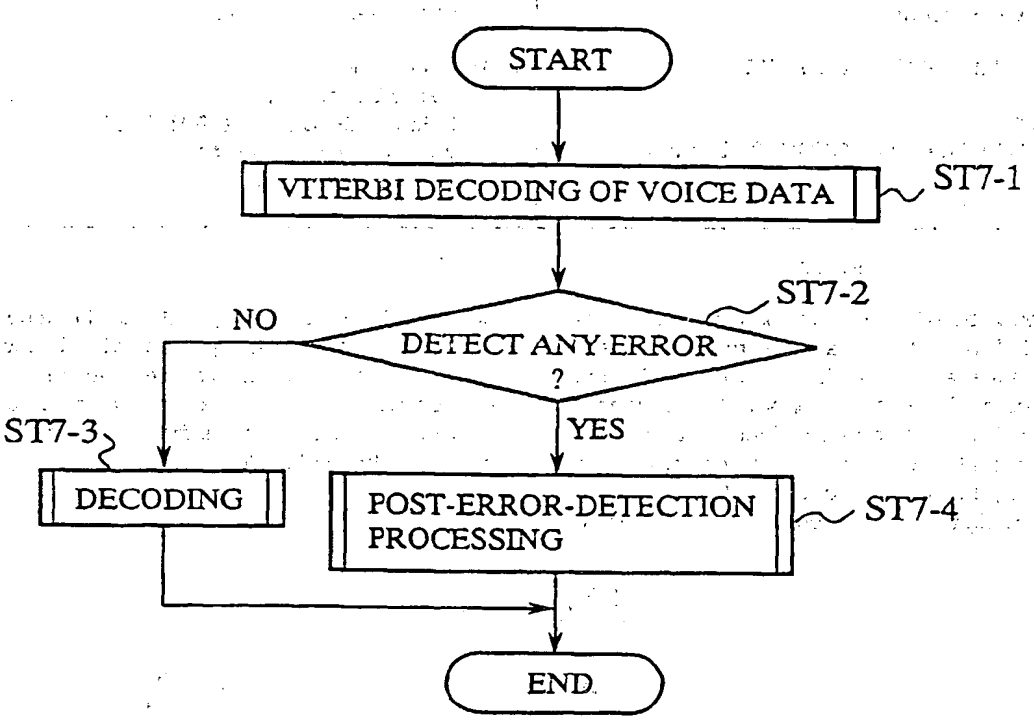

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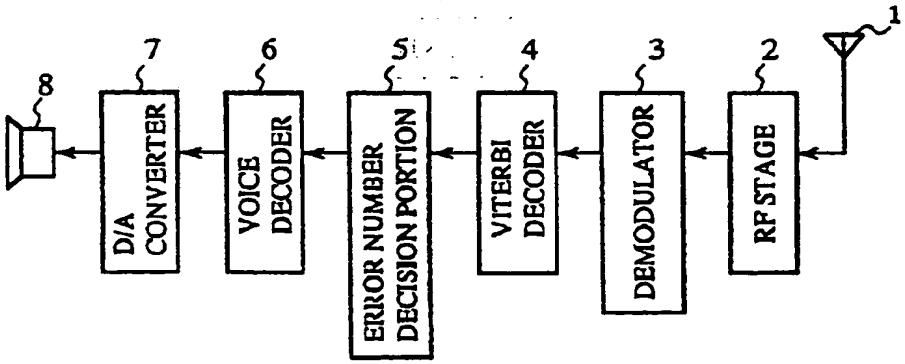
FIG.1



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EUROPEAN SEARCH REPORT

Application Number
EP 97 12 3004

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
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A	---	4,5	
X	EP 0 659 002 A (PHILIPS PATENTVERWALTUNG ;PHILIPS ELECTRONICS NV (NL)) 21 June 1995 (1995-06-21) * page 9, line 40 - page 11, line 35 * * figures 3-5 *	1,2,6	
A	---	4,5	
X	US 5 229 767 A (WINTER ERIC H ET AL) 20 July 1993 (1993-07-20) * column 1, line 11 - line 42 * * column 4, line 30 - line 44 * * column 5, line 62 - column 6, line 17 *	1,6	
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			H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	11 August 2000	Martínez Martínez, V

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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L : document cited for other reasons

& : member of the same patent family, corresponding document

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 97 12 3004

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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11-08-2000

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